

Hindbookcenter



Hind Book Center & Photostat

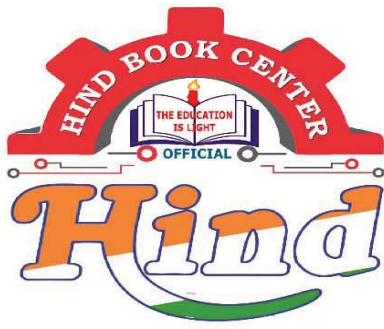
MADE EASY

**Electrical Engineering
Toppers Handwritten Notes
Analog Electronics
BY-A.Rajkumar Sir**

- Colour Print Out
- Blackinwhite Print Out
- Spiral Binding,& Hard Binding
- Test Paper For IES GATE PSUs IAS, CAT,SSC
- All Notes Available & All Book Availabile
- Best Quaity Handwritten Classroom Notes & Study Materials
- IES GATE PSUs IAS CAT Other Competitive/Entrence Exams

Visit us:-www.hindbookcenter.com

**Courier Facility All Over India
(DTDC & INDIA POST)
Mob-9711475393**



Hindbookcenter



ALL NOTES BOOKS AVAILABLE ALL STUDY MATERIAL AVAILABLE
COURIERS SERVICE AVAILABLE

MADE EASY, IES MASTER, ACE ACADEMY, KREATRYX

ESE, GATE, PSUs BEST QUALITY TOPPER HAND WRITTEN NOTES
MINIMUM PRICE AVAILABLE @ OUR WEBSITE

- | | |
|--------------------------------|---------------------------|
| 1. ELECTRONICS ENGINEERING | 2. ELECTRICAL ENGINEERING |
| 3. MECHANICAL ENGINEERING | 4. CIVIL ENGINEERING |
| 5. INSTRUMENTATION ENGINEERING | 6. COMPUTER SCIENCE |

IES, GATE, PSU TEST SERIES AVAILABLE @ OUR WEBSITE

- ❖ IES –PRELIMS & MAINS
- ❖ GATE

➤ NOTE;- ALL ENGINEERING BRANCHS

➤ ALL PSUs PREVIOUS YEAR QUESTION PAPER @ OUR WEBSITE

PUBLICATIONS BOOKS -

MADE EASY, IES MASTER, ACE ACADEMY, KREATRYX, GATE ACADEMY, ARIHANT, GK
RAKESH YADAV, KD CAMPUS, FOUNDATION, MC –GRAW HILL (TMH), PEARSON...OTHERS

HEAVY DISCOUNTS BOOKS AVAILABLE @ OUR WEBSITE

Shop No.7/8 Saidulajab Market Neb Sarai More, Saket, New Delhi-30	Shop No: 46 100 Futa M.G. Rd Near Made Easy Ghitorni, New Delhi-30	F518 Near Kali Maa Mandir Lado Sarai New Delhi-110030	Shop No.7/8 Saidulajab Market Neb Sarai More, Saket, New Delhi-30
--	---	--	--

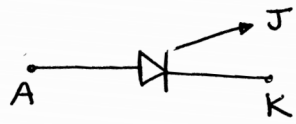
Website: www.hindbookcenter.com

Contact Us: 9711475393

-: Analog Electronics :-

-: Chapter-1 Diode models :-

Ideal model :-



Indication:

A → Anode (+)

K → Cathode (-)

J → Junction

Arrow → unidirectional device

↓
[impedance are different]

conditions for ideal model of diode :-

$V_A - V_K > 0$ then $D = ON$ $\xrightarrow{\text{S.C.}}$ $V_D = 0, I_D > 0$

$V_A - V_K < 0$ then $D = OFF$ $\xrightarrow{\text{O.C.}}$ $V_D = V_B, I_D = 0$

$V_A - V_K = 0$ then D just ON $\xrightarrow{\text{S.C.}}$ $V_D = 0, I_D = 0$

$V_B =$ Battery voltage

Testing method to check diode status :-

a. Short circuit Test (SC Test) [Failure when KVL violates in the ckt]

b. open circuit Test (OC Test) [Failure when KCL violates in the ckt]

Procedure to check diode status using SC Test :-

Rule 1:- Assume all the diodes to be S.C.

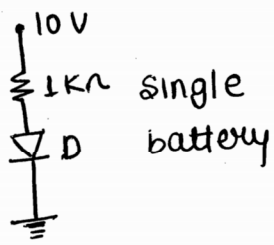
Rule 2:- Indicate the current direction of each diode from A to K.

Rule 3:- check & calculate I_D of each diode by using KVL or KCL

Status: $I_D > 0$; $D = ON$

$I_D < 0$; $D = OFF$

Example 1: Check the status of diode D in the given ckt

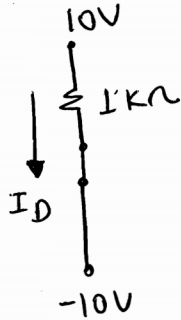


dual battery

Solution:-



⇒

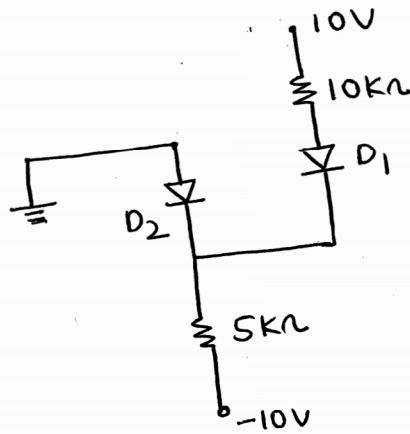


$$I_D = \frac{10 - (-10)}{1K}$$

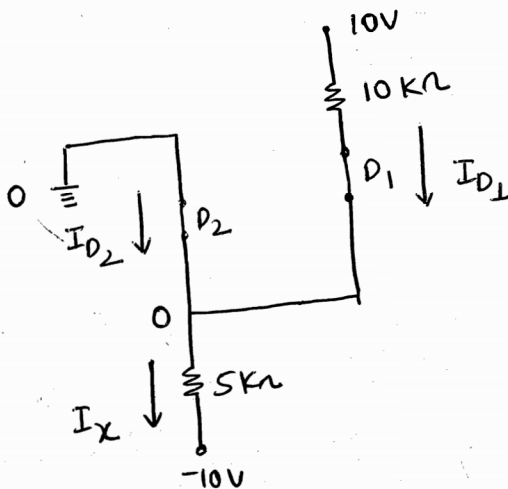
$$= 20\text{mA} > 0$$

↳ D ON

Example 2: Check the status of D_1 & D_2 in the given ckt



Solution:-



$$I_{D1} = \frac{10 - (0)}{10K} = 1\text{mA} > 0$$

↳ D_1 ON

$$I_x = \frac{0 - (-10)}{5K} = 2\text{mA}$$

KCL @ node 'a'

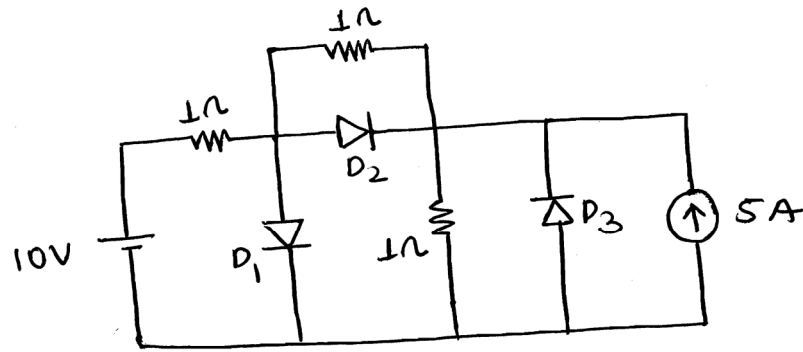
$$I_{D1} + I_{D2} = I_x$$

$$I_{D2} = 2\text{mA} - 1\text{mA}$$

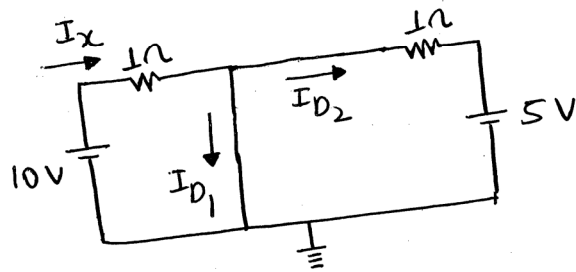
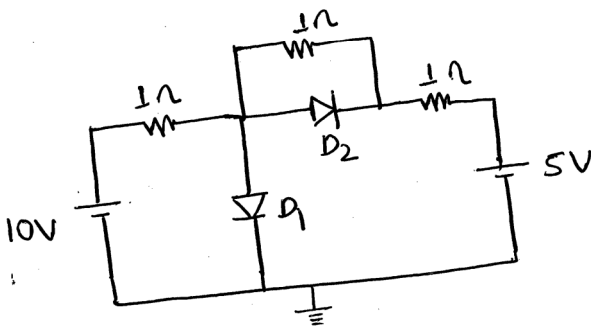
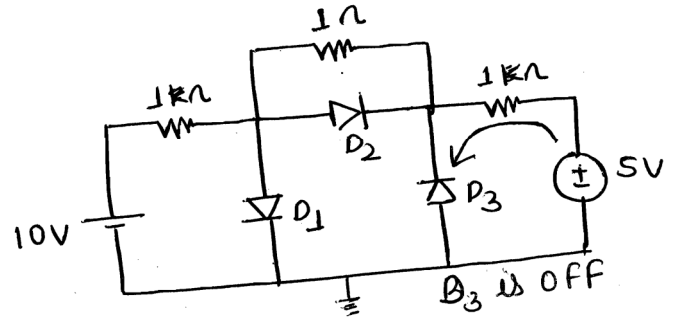
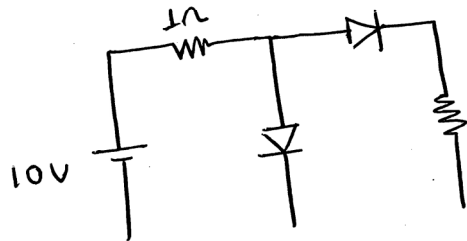
$$I_{D2} = 1\text{mA} > 0$$

↳ D_2 ON

Q.N:- what are the states of the three ideal diodes of the circuit



Solution:-



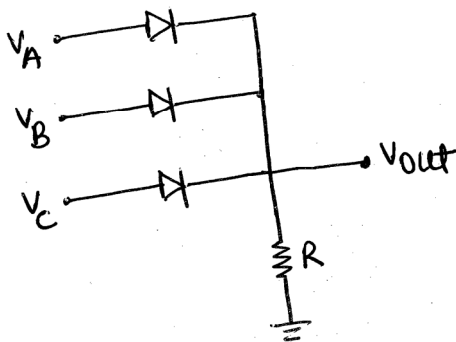
$$I_x = \frac{10-0}{1} = 10A \quad I_{D2} = \frac{0-5}{1} = -5A < 0 \rightarrow D_2 \text{ is OFF}$$

KCL at node a $I_x = I_{D1} + I_{D2}$

$$I_{D1} = 10 - (-5)$$

$$I_{D1} = 15A > 0 \rightarrow D_1 \text{ is ON}$$

Conclusion:-



$$V_A = 5V, V_B = 3V, V_C = 1V$$

Failure of KVL in the short circuit test.
It violates KVL

$$V_{out} = 5V$$

Procedure to check diode status using open circuit test :-

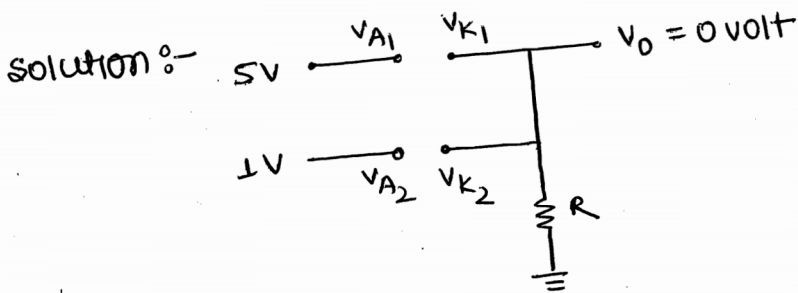
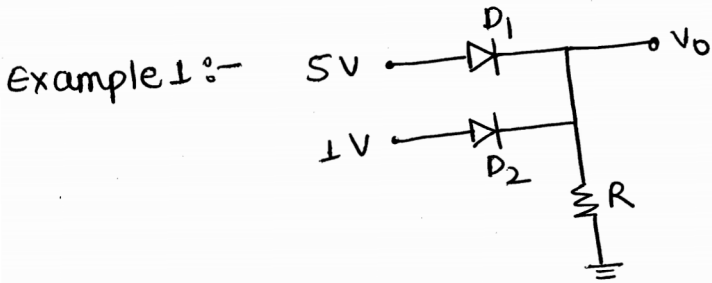
Rule 1: Assume all the diodes to be OFF

Rule 2: Indicate V_A & V_K of each diodes

Rule 3: Calculate $V_A - V_K$ difference of each diodes

Status: $V_A - V_K > 0 \quad D = ON$

$V_A - V_K < 0 \quad D = OFF$

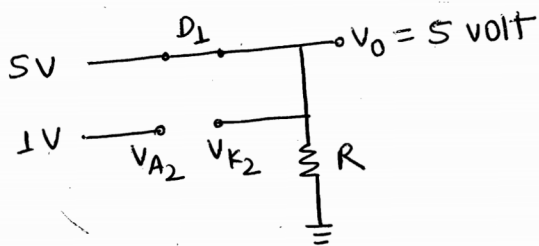


$$V_{A1} - V_{K1} = 5 - 0 = 5 > 0$$

$$V_{A2} - V_{K2} = 1 - 0 = 1 > 0$$

Two diodes ON simultaneously
Then recheck condition

Select D_1 ON first because it is more FB

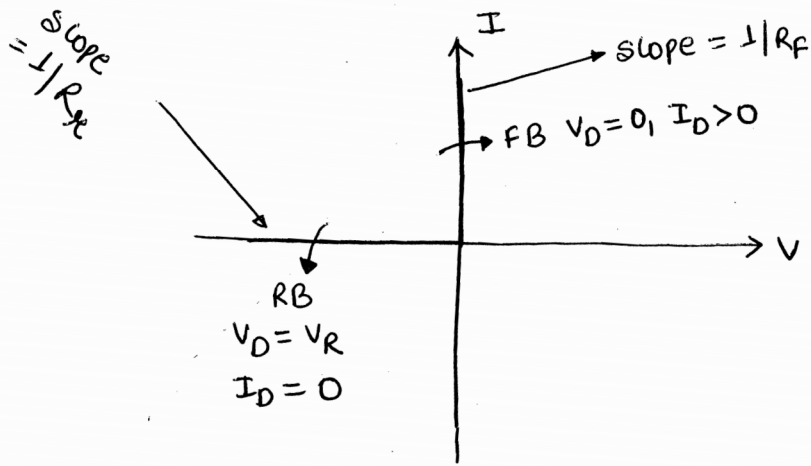


$$V_{A2} - V_{K2} = 1 - 5 = -4 < 0$$

$\rightarrow D_2$ become OFF

Highest voltage will be ON first.

V-I characteristic of ideal diode :-



Indication: R_F = forward diode resistance

R_R = Reverse diode resistance

In forward bias : slope = $\frac{1}{R_F} = \infty \Rightarrow R_F = 0$ ideal diode

In reverse bias : slope = $\frac{1}{R_R} = 0 \Rightarrow R_R = \infty$ ideal diode

CVD model :-

CVD means constant voltage drop model

Practical diode will have cut in voltage V_γ .

V_γ (si) \rightarrow 0.5V to 0.7V

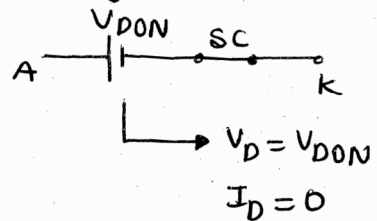
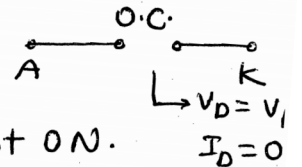
$V_D = V_\gamma$ then $V_D = V_{D,ON}$

condition for CVD model :-

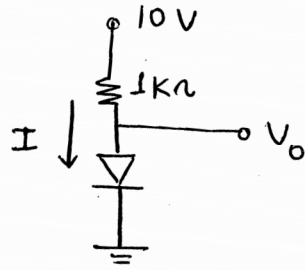
$V_A - V_K > V_{D,ON}$ then D ON

$V_A - V_K < V_{D,ON}$ then D = OFF

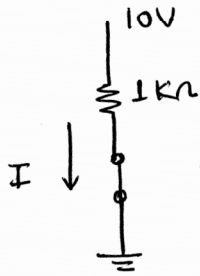
$V_A - V_K = V_{D,ON}$ then D just ON.



EX 1 :- Check the status of diode and calculate V_o and I using Ideal & CVD model.



Solution :- Ideal condition :- [sc Test]

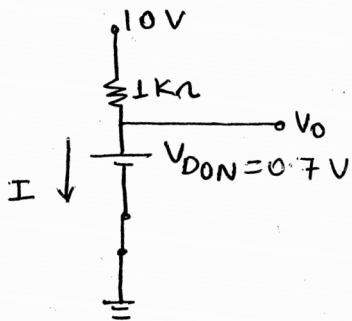


$$I = \frac{10 - 0}{1K}$$

$$= 10\text{mA} > 0 \text{ then } D \text{ ON}$$

$$V = 0, I = 10\text{mA}$$

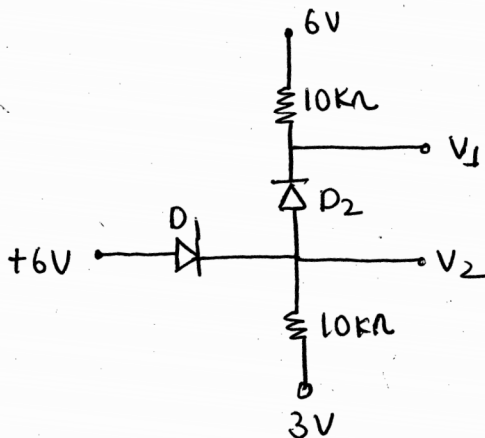
CVD condition :- [sc Test]



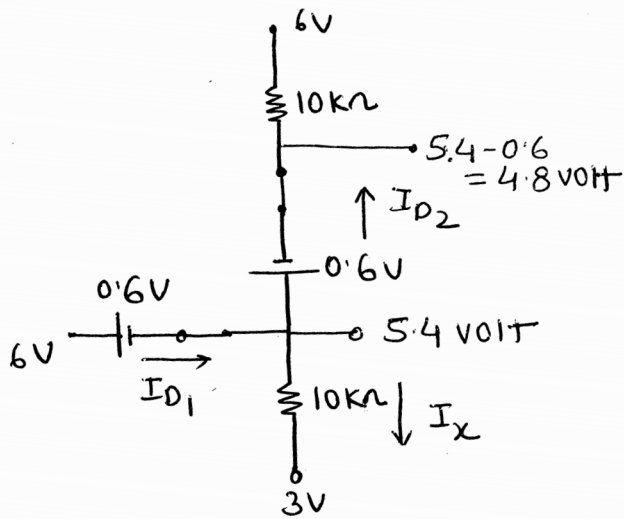
$$I = \frac{10 - 0.7}{1K} = 9.3\text{mA} > 0 \text{ then } D \text{ ON}$$

$$V_o = 0.7\text{VOLT}, I = 9.3\text{mA}$$

Q.N:14 The voltage at V_1 & V_2 of the arrangement shown in figure will be respectively $V_1 = 0.6$ volt



Solution:-



$$I_X = \frac{5.4 - 3}{10K} = 0.24 \text{ mA}$$

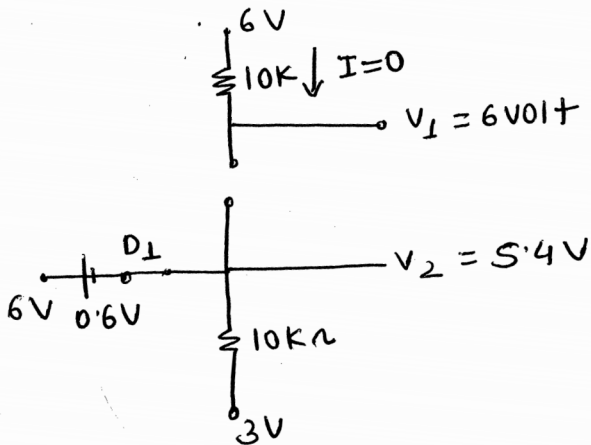
$$I_{D2} = \frac{4.8 - 6}{10K} = -0.12 \text{ mA} < 0$$

↳ D_2 is in OFF condition

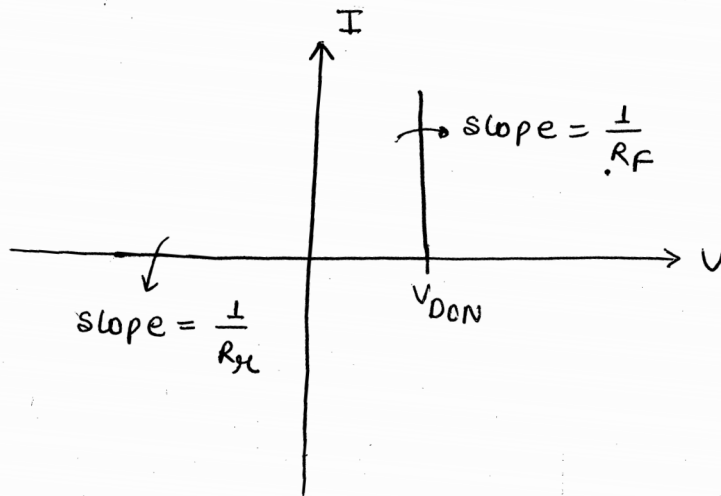
KCL @ 5.4V

$$I_{D1} = I_{D2} + I_X = -0.12 + 0.24 = 0.12 \text{ mA} > 0$$

↳ D_1 is in ON condition



V-I characteristic of CVD model :-



In forward bias slope = $\frac{1}{R_f} = \infty$ $R_f = 0$

In reverse bias slope = $\frac{1}{R_{re}} = 0$ $R_{re} = \infty$

PWL model :-

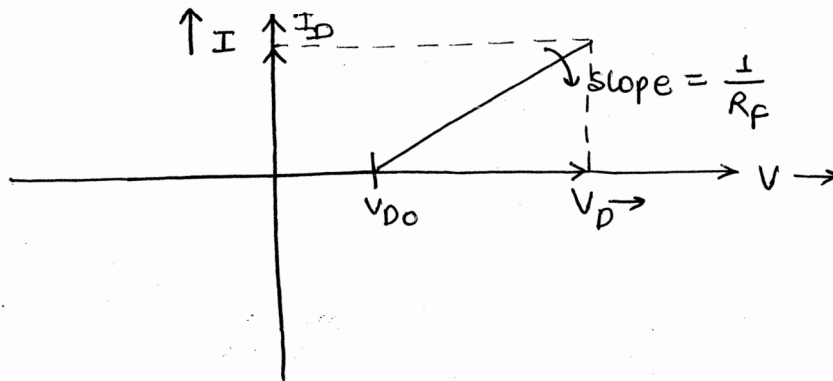
PWL means piece wise linear model

In PWL model : V_{D0} , R_f will be given.

V_{D0} : cut in voltage (V_{D0N})

R_f : forward resistance of diode

V-I characteristic of PWL model :-

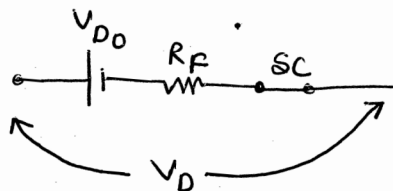


In forward bias slope = $\frac{1}{R_f} = \frac{I_D - 0}{V_D - V_{D0}}$

$$R_f = \frac{V_D - V_{D0}}{I_D}$$

conditions in PWL model :-

$V_A - V_K > V_{D0}$ D = ON



$V_A - V_K < V_{D0}$ D = OFF

